**Discussion notes 23Mar23**

**Progress**:

**Imperas:** Open HW cores run constant ACT testing in the dev cycle.

Five cores going through thru test early in their life; Environment config is up for one

**Chair:** New PR on trap handler up. It replaces LA in trap handler with a pointer table to simplify VM tests,

Simplify privilege mode changes, and simplify cross mode trap signature reporting

**Issues**: **Zfh  PR discussion.**

**Seagate** Need to add canonical list of supported extensions   
(e.g. B & K extensions are mislabeled, A and Zicsr are missing tests,

Seagate ReadMe’s need refactoring to correct and to reduce maintenance)

**Zfh  PR discussion.**

**IITM:**  Need to raise ISAC and CTG PRs before actual tests

* Nan boxing behavior needs to be accurately tested for the Zfh instructions. This can be done by two ways.
  + Always use the entire Freg width, enabling both correct&incorrect NaN-boxed upper half, for all tests
  + Use FP width (halfword) Ld/St for op testing, and develop separate by tests using full width Ld/St for Nan-box specific tests. This is how the PR works (and it set FLEN to operand width).
  + Both must have coverpoints which capture both correct and incorrect Nan-boxed cases.

**Incore**:  It’s easier to do the former. Only need to add incorrectly nan-boxed inputs for the add’l test cases

Macros currently in the repo assume that the FLEN is the width of the register.

**Chair:** Both ways can work; as long as the appropriate coverage is met. (but keep FLEN as register width)

**Zhinx  PR discussion.**

*Floating-point operands of width w < XLEN bits occupy bits w-1:0 of an x register.  
Floating-point operations on w-bit operands ignore operand bits XLEN-1:w.*

*Floating-point operations producing w < XLEN-bit results [sign extend from bit w-1 with copies of bit w-1 (the sign bit).*

**Incore** Zfinx coverpoints do not capture the “ignore upper bits” constraint mentioned in the spec

* + The coverpoints need to have accurate conditions defined on this. E.g. rs2[XLEN-1:0] == 0
  + The tests need to be testing for this ignore behavior. Need additional tests and coverpoints
  + Should either store the entire reg or account for cross product of all input classes X prefix values in some test

**Incore**: Better to load and store the entire register in both cases by default.   
These problems have already been addressed in the macros. Will save time.

**Seagate** – List of extensions supported in the Suite. Extensions like B and K are put in consolidated directories. Need sub-extension specific categorization. Need zicsr(Issue #316) opcode tests. Could probably use mscratch to test these (because it must always be fully RW in appropriate mode, and HW never writes it)

Note that results of halfword ops always return a canonical NaN, so need to store the entire word to ensure that is done correctly (for each op class).

The was a discussion about how Spike and Sail were handling NaNs incorrectly, but it appears to have been a test issue. Zfh always Nan-boxes results and checks NaN-Boxing on inputs, which zhinx always ignores NaN boxed inputs, and always generates signed extended (but not NaN-boxed) results (which are different than NAnBoxed when the result is positive)